In the Claims

1. (Currently Amended) A switch comprising:

a plurality of field effect transistors connected in series, each field effect transistor including a gate, a source, and a drain, each gate having a gate width and a gate length;

said gate length of one of said series connected field effect transistors being a different size from said gate length of another series connected field effect transistor.

2. (Currently Amended) The switch as claimed in claim 1, wherein said gate of one of said plurality of series connected field effect transistor has a longer gate length ~~and/or gate width~~ than said gate of said other series connected field effect transistor.

3. (Original) The switch as claimed in claim 1, wherein said gate of one of said plurality of series connected field effect transistor has a distance to its drain port that is less than a distance to its source port.

4. (Original) The switch as claimed in claim 1, wherein said gate of one of said plurality of series connected field effect transistor has a distance to its source port that is less than a distance to its drain port.

5. (Original) The switch as claimed in claim 3, wherein said gate of said other series connected field effect transistor has a distance to its source port that is equal to a distance to its drain port.

6. (Original) The switch as claimed in claim 4, wherein said gate of said other series connected field effect transistor has a distance to its source port that is equal to a distance to its drain port.

7. (Original) The switch as claimed in claim 1, wherein the different gate sizes increase a parasitic capacitance within the switch.

8. (Original) A switch comprising:

a plurality of dual-gate field effect transistors connected in series, each dual-gate field effect transistor including two gates, a source, and a drain;

one of said series connected dual-gate field effect transistors having a modified gate therein that is of a different size from gates of other series connected dual-gate field effect transistors.

9. (Original) The switch as claimed in claim 8, wherein said modified gate of said series connected dual-gate field effect transistor has a longer gate length and/or gate width than gates of said other series connected dual-gate field effect transistor.

10. (Original) The switch as claimed in claim 8, wherein said modified gate of said series connected dual-gate field effect transistor has a distance to its drain port that is less than a distance to its source port.

11. (Original) The switch as claimed in claim 8, wherein said modified gate of said series connected dual-gate field effect transistor has a distance to its source port that is less than a distance to its drain port.

12. (Original) The switch as claimed in claim 10, wherein gates of said other series connected dual-gate field effect transistors have a distance to its source port that is equal to a distance to its drain port.

13. (Original) The switch as claimed in claim 11, wherein gates of said other series connected dual-gate field effect transistors have a distance to its source port that is equal to a distance to its drain port.

14. (Original) The switch as claimed in claim 8, wherein a second series connected dual-gate field effect transistor has a modified gate therein that is of a different size from gates of other series connected dual-gate field effect transistors.

15. (Original) The switch as claimed in claim 8, wherein said dual-gate field effect transistors are high-electron-mobility-transistors.

16. (Original) The switch as claimed in claim 8, wherein the different gate sizes increase a parasitic capacitance within the switch.

17. (Original) The switch as claimed in claim 8, wherein said dual-gate field effect transistors include a transistor connection segment between said gates and a heavily doped cap layer fabricated upon said transistor connection segment between said gates.

Claim18 (Cancelled)

19. (Currently Amended) A ~~The~~ high-electron-mobility-transistor ~~as claimed in claim 18~~, comprising:

two gate fingers;

a transistor connection segment between said gate fingers; and

a heavily doped cap layer fabricated upon said transistor connection segment between said gate fingers; ~~wherein~~

said gate fingers being ~~are~~ of different sizes.

20. (Original) The high-electron-mobility-transistor as claimed in claim 19, wherein one of said gate fingers has a distance to its source port that is less than a distance to its drain port.

21. (Original) The high-electron-mobility-transistor as claimed in claim 19, wherein one of said gate fingers has a distance to its drain port that is less than a distance to its source port.

22. (Original) A radio frequency single pole double throw switch, comprising:

a receiver port;

a transmitter port;

an antenna port;

a receiver section connecting said receiver port to said antenna; and

a transmitter section connecting said transmitter port to said antenna;

said receiver section including a plurality of dual-gate field effect transistors connected in series, each dual-gate field effect transistor including two gates, a source, and a drain such that

one of said series connected dual-gate field effect transistors has a modified gate therein that is of a different size from gates of other series connected dual-gate field effect transistors.

23. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein a source of said modified gate transistor is connected to said receiver port.

24. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein a drain of said modified gate transistor is connected to said antenna port.

25. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein a second series connected dual-gate field effect transistor has a second modified gate therein that is of a different size from gates of other series connected dual-gate field effect transistors.

26. (Original) The radio frequency single pole double throw switch as claimed in claim 25, wherein a source of said modified gate transistor is connected to said receiver port and a drain of said second modified gate transistor is connected to said antenna port.

27. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein said dual-gate field effect transistors are high-electron-mobility-transistors.

28. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein said modified gate of said series connected dual-gate field effect transistor has a longer gate length and/or gate width than gates of said other series connected dual-gate field effect transistor.

29. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein said modified gate of said series connected dual-gate field effect transistor has a distance to its drain port that is less than a distance to its source port.

30. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein said modified gate of said series connected dual-gate field effect transistor has a distance to its source port that is less than a distance to its drain port.

31. (Original) The radio frequency single pole double throw switch as claimed in claim 29, wherein gates of said other series connected dual-gate field effect transistors have a distance to its source port that is equal to a distance to its drain port.

32. (Original) The radio frequency single pole double throw switch as claimed in claim 30, wherein gates of said other series connected dual-gate field effect transistors have a distance to its source port that is equal to a distance to its drain port.

33. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein the different gate sizes increase a parasitic capacitance within the switch.

34. (Original) The radio frequency single pole double throw switch as claimed in claim 22, wherein said dual-gate field effect transistors include a transistor connection segment between said gates and a heavily doped cap layer fabricated upon said transistor connection segment between said gates.

35. (Currently Amended) A radio frequency single pole double throw switch, comprising:

a receiver port;

a transmitter port;

an antenna port;

a receiver section connecting said receiver port to said antenna; and

a transmitter section connecting said transmitter port to said antenna;

said receiver section ~~including a plurality of field effect transistors connected in series, each field effect transistor including a gate, a source, and a drain such that one of said series connected field effect transistors has a modified gate therein that is a different size from said gate of another series connected field effect transistor~~ including,

a first receiver dual-gate high electron mobility transistor having gates of different lengths, and

a second receiver dual-gate high electron mobility transistor having gates of different lengths.

36. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein the source of said first receiver dual-gate high electron mobility ~~modified gate~~ transistor is connected to said receiver port.

37. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein the drain of said second receiver dual-gate high electron mobility ~~modified gate~~ transistor is connected to said antenna port.

38. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein ~~a second series connected field effect transistors has a second modified gate therein that is of a different size from gates of other series connected field effect transistors~~ said transmitter section includes a first transmitter dual-gate high electron mobility transistor having gates of different lengths and a second transmitter dual-gate high electron mobility transistor having gates of different lengths.

39. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 38, wherein the source of said first transmitter dual-gate high electron mobility ~~modified gate~~ transistor is connected to said receiver port and the drain of said second transmitter dual-gate high electron mobility ~~modified gate~~ transistor is connected to said antenna port.

40. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein a first ~~said modified~~ gate of said first receiver dual-gate high electron mobility transistor ~~series connected field effect transistor~~ has a longer gate length and/or gate width than ~~gates of said other series connected field effect transistor~~ a second gate of said first receiver dual-gate high electron mobility transistor.

41. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein a first ~~said modified~~ gate of said first receiver dual-gate high electron mobility transistor ~~series connected field effect transistor~~ has a distance to its drain port that is less than a distance to its source port.

42. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein a first ~~said modified~~ gate of said second receiver dual-gate high electron mobility transistor ~~series-connected field-effect transistor~~ has a distance to its source port that is less than a distance to its drain port.

Cancelled Claims 43-44

45. (Currently Amended) The radio frequency single pole double throw switch as claimed in claim 35, wherein the different gate ~~sizes~~ lengths increase a parasitic capacitance within the switch.

46. (Currently Amended) The radio frequency single pole double throw switch claimed in claim 35, wherein the different gate ~~sizes~~ lengths improve the linearity without impacting the ESD and EOS ruggedness.

47. (New) A series connected dual-gate transistor, comprising:

a first gate; and

a second gate;

said first gate having a gate width and a gate length;

said second gate having a gate width and a gate length;

said gate length of said first gate being a different size from said gate length of said second gate.

48. (New) The series connected dual-gate transistor as claimed in claim 47, wherein said said gate width of said first gate being a different size from said gate width of said second gate.

49. (New) A dual-gate transistor having gates with different size lengths.

50. (New) A dual-gate transistor having gates with different size lengths, the gates having different size widths.